REMARKS

Applicant affirms the election of Group I, including claims 1-3. Claims 4-5 are canceled above as being directed to a non-elected invention without prejudice to the filing of divisional or continuation applications.

Claims 1-3 are rejected as being anticipated by Shin (U.S. Patent No. 6,342,801). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections are respectfully requested.

The applicant's invention is directed to a duty cycle correction circuit of a delay locked loop comprising a current control circuit. The current control circuit controls an amount of electric charge accumulated in a first storage unit and an amount of electric charge accumulated in a second storage unit, in response to a combination of duty cycle switching signals and corresponding current switching control signals.

This feature is illustrated by way of example at least at FIG. 3 of the present specification. In this example, a current control circuit 237 controls an amount of electric charge accumulated in a first storage unit N55 and second storage unit N57 in response to duty cycle switching signals DN, UP, and current switching control signals CNTL1, CNTL2, ... ,CNTLN. Signals DN, UP are duty cycle switching signals for decreasing and increasing the duty rate, respectively. Specifically, the amounts of electric charge accumulated in the first storage unit N55 and the second storage unit N57 are adjusted by applying a combination of the duty cycle switching signal UP and the respective current switching control signals CNTL1, CNTL2, ... ,CNTLN to increase the duty rate, or by applying a combination of the duty cycle switching signal DN and the respective current switching control signals CNTL1, CNTL2, ... ,CNTLN to decrease the duty rate.

Shin discloses a duty cycle correction circuit of a delay locked loop circuit in a Rambus DRAM (see Shin Abstract, and page 9, lines 48-49). The Rambus DRAM includes a normal mode and a power save mode, wherein the power save includes a nap mode and a power down

mode (see Shin, column 1, lines 30-32). The Shin invention compulsorily corrects the capacitance of a storage capacitor lost during the transition from the power save mode to the normal mode (see Shin, column 9, lines 31-40). This is achieved by applying a control signal pdn to transistors P13, P15, each transistor P13, P15 connected to a corresponding storage capacitor N23, N27, wherein the control signal pdn controls the power supply voltage VddA to each respective storage capacitor N23, N27 (see Shin, Figure 5 and column 8, lines 36-38).

It is submitted that Shin fails to teach or suggest the present invention. In particular, it is submitted that Shin fails to teach or suggest a current control circuit which controls an amount of electric charge accumulated in a first storage unit and an amount of electric charge accumulated in a second storage unit, in response to a combination of duty cycle switching signals and corresponding current switching control signals, as claimed. The Office Action cites the control signal pdn of Shin as being a corresponding switching control signal. However, the control signal pdn of Shin is generated when the duty cycle correction circuit 430 transitions from the power save mode to a normal mode. There is no mention in Shin of a combination of duty cycle switching signals and corresponding current switching control signals being used to control an amount of electric charge accumulated in either the first storage unit or second storage unit, as clamed. Moreover, Shin discloses a single control signal, i.e., the pdn signal, to correct the capacitance of a storage capacitor lost during the transition from the power save mode to the normal mode.

For these reasons, it is submitted that Shin fails to teach or suggest the present invention set forth in the amended claims. Reconsideration of the rejections of claims 1-3 under 35 U.S.C. 102(b) based on Shin is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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